80386
FOUNDATION FOR INNOVATIVE PRODUCTS
OVERVIEW
80386 OVERVIEW
FULL 32-BIT ARCHITECTURE

EXECUTION UNIT
- 32-BIT REGISTER FILE
- BARREL SHIFTER
- ALU

SEGMENT UNIT
- SEGMENT DESCRIPTOR CACHE

PAGING UNIT
- PAGE DESCRIPTOR CACHE

INSTRUCTION QUEUE
INSTRUCTION UNIT
INSTRUCTION DECODE UNIT

PRE-FETCH QUEUE
PRE-FETCH UNIT

CODE PREFETCH UNIT

BUS UNIT
BUS INTERFACE UNIT

32-BIT ADDRESS BUS
32-BIT DATA BUS

FLEXIBLE ON-CHIP MEMORY MANAGEMENT
- 32-BIT REGISTERS
- 32-BIT BUS
- 32-BIT INSTRUCTION SET
- 32-BIT ADDRESSING MODES
INTERNAL PIPELINING
THE FOUNDATION FOR PERFORMANCE

- PARALLEL OPERATION
  - FETCHING
  - DECODING
  - EXECUTION
  - ADDRESS TRANSLATING

32-BIT ADDRESS BUS

32-BIT DATA BUS
INTERNAL PIPELINING
80386 PREFETCH UNIT

- PREFETCHES INSTRUCTIONS
- 16 BYTES OF PREFETCHED INSTRUCTIONS
INTERNAL PIPELINING
80386 BUS INTERFACE UNIT

- DEMULTIPLEXED FOR HIGHER PERFORMANCE
  - 32 MegaByte/SEC TRANSFER RATE
- 1.5-3X FASTER THAN COMPETITORS
80386 OVERVIEW
PROGRAM ADDRESS SPACE

EXECUTION UNIT
- 32-BIT REGISTER FILE
- BARREL SHIFTER
- ALU

SEGMENT UNIT
- SEGMENT DESCRIPTOR CACHE

PAGING UNIT
- PAGE DESCRIPTOR CACHE

INSTRUCTION QUEUE

INSTRUCTION UNIT

INSTRUCTION DECODE UNIT

PRE-FETCH QUEUE

CODE PREFETCH UNIT

BUS UNIT

BUS INTERFACE UNIT

32-BIT ADDRESS BUS

32-BIT DATA BUS

FLEXIBLE ON-CHIP MEMORY MANAGEMENT
- 4 GBYTE FLAT
- 64 TBYTE SEGMENTED AND PAGED
- 1 BYTE SEGMENTS
- 4 GBYTE SEGMENTS
INTERNAL PIPELINING
80386 SEGMENTATION UNIT

- PERFORMS EFFECTIVE ADDRESS CALCULATIONS
- PERFORMS PROTECTION CHECKS
- 32-BIT ADDERS & SHIFTERS
- EFFECTIVE ADDRESS CALCULATION: 0/1 CLOCKS
- CACHE OF SEGMENT INFORMATION ALLOWS OVERLAPPED PROTECTION CHECKING
INTERNAL PIPELINING
80386 PAGING UNIT

- Translates linear addresses to physical addresses
- Pipelined with other operations
- Contains an address translation cache (TLB) of 32 page table entries
- > 98% hit rate for memory accesses

Demand paging without performance penalties
80386 OVERVIEW
COMPUTATION MODEL

RANGE OF CAPABILITY
- FAST CORE INSTRUCTIONS
- REGISTER ADDRESSING
- BIT DATA TYPE

OPERATING SYSTEM AND HIGH LEVEL LANGUAGE INSTRUCTIONS
4-COMPONENT ADDRESSING
EXTENDED FLOATING POINT DATA TYPE
INTERNAL PIPELINING
80386 INSTRUCTION DECODE UNIT

- TRANSLATES OPCODES TO INTERNAL FORMAT
- CONTAINS QUEUE OF 3 FULLY DECODED INSTRUCTIONS
- ALLOWS EARLY STARTING OF EFFECTIVE ADDRESS CALCULATION
- FULLY HIDES INSTRUCTION DECODE TIME
INTERNAL PIPELINING
80386 EXECUTION UNIT

- PERFORMS ALL ARITHMETIC OPERATIONS IN ONE CLOCK
- CONTAINS 64-BIT BARREL SHIFTER
  - ROTATES ANY NUMBER OF BITS IN ONE CLOCK
  - ACCELERATES SHIFT, ROTATE, MULTIPLY AND BIT FIELD INSTRUCTIONS
- 1-3X THE COMPETITION
INTERNAL PIPELINING
THE FOUNDATION FOR PERFORMANCE

80386:
VIRTUAL ADDRESS

EA CALCULATION:
0-1 CLOCKS
(TYPICAL: 0)

LINEAR ADDRESS

PAGING
(PIPELINED)
0-1 CLOCKS
(TYPICAL: 1/2 CLOCK)

PHYSICAL ADDRESS

BRAND M:
0-24 CLOCKS
TYPICAL 4.2

1 OR MORE
WAIT-STATES

- FULL VIRTUAL TO PHYSICAL ADDRESS TRANSLATION WITH NO OVERHEAD
- TYPICALLY 5+ CLOCKS FASTER THAN "BRAND M"
80386 OVERVIEW
HARDWARE CONFIGURATION OPTIONS

• FLEXIBLE BUS
  - DYNAMIC RAM
  - FAST MEMORY
  - CACHE MEMORY
  - DYNAMIC BUS SIZING

• COPROCESSOR INTERFACE
  - 16 BIT COPROCESSOR
  - 32 BIT COPROCESSOR

• PROCESSOR SELF-TEST

• BUILT-IN SUPPORT FOR BOARD TEST
HARDWARE OVERVIEW
HARDWARE OVERVIEW
AGENDA

- INTRODUCTION
- BUS
- MEMORY DESIGN
- CACHE CAPABILITY
- NUMERICS
INTRODUCTION
80386 SYSTEM BLOCK DIAGRAM

82384 CLOCK

A<sub>31</sub> - A<sub>0</sub>
80386 CPU
D<sub>31</sub> - D<sub>0</sub>

SUPPORT HARDWARE

CACHE
MAIN MEMORY

ADDRESS BUS
DATA BUS

32 MHZ

OPTIONAL FLOATING POINT COPROCESSOR
INTRODUCTION

80386 PIN OUT

• 132 PIN PGA

• 41 POWER AND GROUND PINS FOR CLEAN HIGH FREQUENCY OPERATION
INTRODUCTION
80386 BLOCK DIAGRAM

32 MHz
82384
CLOCK

32-BIT DATA { DO-D31 } DATA BUS

BUS CONTROL

BUS ARBITRATION

INTERRUPTS

CLK2

ADDRESS BUS

A2-A31

BYTE ENABLES

32-BIT ADDRESS

BUS CYCLE DEFINITION

COPROCESSOR SIGNALLING

POWER CONNECTION

80386 PROCESSOR

ADS#
NA#
BS16#
READY#
HOLD
HLDA
INTR
NMI
RESET

BE3#
BE2#
BE1#
BE0#
W/R#
D/C#
M/IO
LOCK#
PEREQ
BUSY#
ERROR#
Vcc
GND
HARDWARE OVERVIEW
AGENDA

- INTRODUCTION
- BUS
- MEMORY DESIGN
- CACHE CAPABILITY
- NUMERICS
80386 HIGH SPEED BUS

• 32-BIT ADDRESS BUS

• 32-BIT DATA BUS

• 32 MEGABYTES PER SECOND AT 16MHz

• DESIGNED FOR PERFORMANCE AND FLEXIBILITY
  - 2 CLOCK HIGH PERFORMANCE BUS
  - OPTIONAL PIPELINING FOR MAXIMUM PERFORMANCE WITH LOW COST MEMORY
  - DYNAMIC BUS SIZING
80386 HIGH SPEED BUS
2 CLOCK BUS FOR MAXIMUM PERFORMANCE

- FOR USE WITH HIGH SPEED MEMORIES AND CACHES
- 0 WAIT STATE MEMORY REQUIREMENT

(2) X 62.5 NSec CLOCK         125 NSec
ADDRESS OUTPUT DELAY          - 40 NSec
DATA INPUT SETUP TIME         - 10 NSec
                               75 NSec
80386 HIGH SPEED BUS
ADDRESS PIPELINING

- EARLY ADDRESS PROVIDES 1 EXTRA CLOCK OF ACCESS TIME

- MAINTAINS HIGH BANDWIDTH WITH SLOWER MEMORIES:
  - EARLY ADDRESS HIDES DECODE AND PROPAGATION DELAYS
  - 3 CLOCK ADDRESS TO DATA
  - 32 MB/S BANDWIDTH

- NEXT ADDRESS (NA) PIN FOR DYNAMIC PIPELINING ENABLE/DISABLE
  - MAXIMUM FLEXIBILITY FOR BUS CYCLE SELECTION
80386 HIGH SPEED BUS
PIPELINED BUS

- BUS BANDWIDTH
  - 2 CLOCK (32 Mbyte/Sec @ 16 MHz) FOR SEQUENTIAL REFERENCES
  - 3 CLOCK (22.2 Mbyte/Sec @ 16 MHz) FOR NON-SEQUENTIAL REFERENCES

- OPTIMAL FOR USE WITH SLOWER INTERLEAVED DRAM MEMORY
80386 HIGH SPEED BUS
PIPELINED BUS

- 0 WAIT STATE MEMORY REQUIREMENT

(3) X 62.5 NSec CLOCK 187.5 NSec
ADDRESS OUTPUT DELAY - 40 NSec
DATA INPUT SET-UP TIME - 10 NSec

137.5 NSec
80386 HIGH SPEED BUS
DYNAMIC BUS SIZING

- MIXED 16 AND 32-BIT BUS CYCLES
- SUPPORTS 16 AND 32-BIT BUSSSES AND PERIPHERALS
HARDWARE OVERVIEW
AGENDA

• INTRODUCTION
• BUS
• MEMORY DESIGN
• CACHE CAPABILITY
• NUMERICS
80386 MEMORY DESIGN
DYNAMIC RAM

- USES PIPELINING
- USES TWO-BANK INTERLEAVED MEMORY
80386 MEMORY DESIGN
MEMORY SUBSYSTEM

80386

DATA BUS
32

ADDRESS

MEMORY CONTROL

LATCH

DRAM BANK0

A2

LATCH

DRAM BANK1

32

A2

32

TWO BANKS INTERLEAVED
80386 MEMORY DESIGN
PIPELINED BUS OPTION

ADDRESS

DATA
HARDWARE OVERVIEW
AGENDA

• INTRODUCTION
• BUS
• MEMORY DESIGN
• CACHE CAPABILITY
• NUMERICS
CACHE CAPABILITY
PURPOSE

MAKING

INEXPENSIVE
DYNAMIC
RAM

FAST STATIC
RAM

LOOK LIKE

FAST STATIC
RAM
CACHE CAPABILITY
MEMORY SYSTEM PERFORMANCE OPTIMIZATION

- COUPLE FAST MEMORY & SPECIAL CONTROL LOGIC TO SLOWER MAIN MEMORY
- COST APPROACHES SLOW MAIN MEMORY
- SPEED APPROACHES FAST CACHE MEMORY
CACHE CAPABILITY
OVERVIEW

- COMPARE CURRENT ADDRESS WITH ADDRESS TAGS IN CACHE
- IF FOUND (CACHE HIT) READ FROM CACHE
- NOT FOUND (CACHE/MISS) READ FROM MAIN MEMORY, UPDATE CACHE
- DESIGN GOAL: ACCESS CACHE MAJORITY OF THE TIME
CACHE CAPABILITY
FACTORS THAT IMPACT CACHE EFFECTIVENESS

- CACHE SIZE
- BUS BANDWIDTH
- CACHE CONTENTS
  - CODE
  - DATA
  - STACK
CACHE CAPABILITY
80386 CACHE BLOCK DIAGRAM

- 32K TO 64K CACHE YIELDS > 90% HIT RATE
CACHE CAPABILITY
WHY IS THE 80386 GOOD FOR CACHING?

- UNLIMITED CACHE SIZE (UP TO 4 GIGABYTES)
- FULL 32 MBYTES/SEC BUS BANDWIDTH
- NO RESTRICTION ON CONTENTS
  - CODE AND DATA AND STACK
HARDWARE OVERVIEW
AGENDA

• INTRODUCTION
• BUS
• MEMORY DESIGN
• CACHE CAPABILITY
• NUMERICS
80386 NUMERICS
80287 COPROCESSOR

- COST EFFECTIVE NUMERIC COPROCESSOR, AVAILABLE NOW
- 6, 8, AND 10 MHZ SPEED SELECTIONS
- SOFTWARE COMPATIBLE WITH LARGE BASE OF 8087 SOFTWARE
- CAN USE 80387 TO PROTOTYPE FOR 80387 DESIGNS
- IEEE 754 COMPATIBLE
80386 NUMERICS
80387 COPROCESSOR

- COMPLETELY SOFTWARE COMPATIBLE WITH 8087 AND 80287
- HIGH PERFORMANCE: 1.8 MWHETSTONES AT 16 MHz
- ENHANCES TRIGNOMETRIC FUNCTIONS
  - SIN, COS, SIMULTANEOUS SIN/COS
- FULL IEEE 754 IMPLEMENTATION
80386 HARDWARE OVERVIEW
PERIPHERAL SUPPORT

- COMPATIBLE WITH INTEL'S FULL LINE OF PERIPHERALS & COPROCESSORS
80386 HARDWARE OVERVIEW
SUMMARY

- 2-CLOCK BUS CYCLE FOR THE HIGHEST THROUGHPUT
- PIPELINED BUS OPERATION FOR HIGH PERFORMANCE DRAM SYSTEMS
- DYNAMIC BUS SIZING TO SUPPORT MIXES OF 16- AND 32-BIT HARDWARE SUB-SYSTEMS
- MMU ON-CHIP FOR PERFORMANCE AND DESIGN EASE
- RANGE OF NUMERIC COPROCESSORS TO FIT ANY APPLICATION
- COMPATIBLE WITH INTEL'S LARGE FAMILY OF PERIPHERALS
DEBUG AND TEST
DEBUG AND TEST SIMPLIFIED

- ON CHIP DEBUG
- INTEGRATED TEST
80386 ON-CHIP DEBUG DEBUG RESOURCES

• INSTRUCTION SINGLE STEP
• SINGLE BYTE TRAP
• DEBUG REGISTERS
80386 ON-CHIP DEBUG
INSTRUCTION SINGLE STEP

• AUTOMATIC INTERRUPT TO SINGLE STEP HANDLER AFTER EACH INSTRUCTION

• INSTRUCTION BY INSTRUCTION EXECUTION

• ALLOWS INSTRUCTION TRACE
80386 ON-CHIP DEBUG
SINGLE BYTE TRAP

- 1 BYTE OPCODE INSERTED IN INSTRUCTION STREAM
- AUTOMATIC TRAP TO DEBUGGER
- RAM-BASED CODE ONLY
- UNLIMITED NUMBER OF SOFTWARE BREAKPOINTS
### 80386 ON-CHIP DEBUG

#### DEBUG REGISTERS

<table>
<thead>
<tr>
<th>31</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BREAKPOINT 0 LINEAR ADDRESS</strong></td>
<td>DR0</td>
</tr>
<tr>
<td><strong>BREAKPOINT 1 LINEAR ADDRESS</strong></td>
<td>DR1</td>
</tr>
<tr>
<td><strong>BREAKPOINT 2 LINEAR ADDRESS</strong></td>
<td>DR2</td>
</tr>
<tr>
<td><strong>BREAKPOINT 3 LINEAR ADDRESS</strong></td>
<td>DR3</td>
</tr>
<tr>
<td><strong>RESERVED</strong></td>
<td>DR4</td>
</tr>
<tr>
<td><strong>RESERVED</strong></td>
<td>DR5</td>
</tr>
<tr>
<td><strong>STATUS/CONTROL</strong></td>
<td>DR6</td>
</tr>
<tr>
<td><strong>STATUS/CONTROL</strong></td>
<td>DR7</td>
</tr>
</tbody>
</table>

- UP TO 4 HARDWARE BREAKPOINTS
- SUPPORTS SYSTEM WIDE OR TASK SPECIFIC BREAKPOINTS
- SUPPORTS RAM/ROM BREAKPOINTS
- SUPPORTS INSTRUCTION/DATA BREAKPOINTS
80386 ON-CHIP TEST
SIMPLIFY CPU AND BOARD DIAGNOSTICS

• CHIP-LEVEL SELF-TEST

• BOARD-LEVEL TEST HOOKS
80386 ON-CHIP TEST

- TESTS OVER 120,000 TRANSISTORS
  - MICROCODE ROM
  - PROGRAMMABLE ARRAY LOGIC

- SUPPORTS GO- NO/GO DIAGNOSTICS

- REDUCES INCOMING INSPECTION TEST TIME

- ALLOWS FIELD RELIABILITY CHECKS
80386 DOCUMENTATION

AVAILABLE NOW:

- 80386 DATA SHEET
- 82384 DATA SHEET
- 80287 DATA SHEET
- 80387 DATA SHEET
- 1167 SPECIFICATION
- INTRODUCTION TO 80386
- 80386 PROGRAMMER’S REFERENCE MANUAL
- 80386 HARDWARE REFERENCE MANUAL
- 80386 SYSTEM SOFTWARE WRITER’S GUIDE
- 80386 SYSTEM DESIGN APPLICATION NOTE
DEBUG SUPPORT
80386 DEBUG TOOLS

● DEBUG TOOLS FOR ALL PHASES OF DEVELOPMENT
  - ICE™-386 FOR H/W DEVELOPMENT AND HW/SW INTEGRATION
  - PSCOPE MONITOR 80386 (P-MON) FOR SOFTWARE DEVELOPMENT

● UNIFIED SET OF TOOLS
  - CLOSE INTEGRATION WITH INTEL ASSEMBLERS/COMPILERS
  - MULTIPLE 80386 TOOL CONTROL FROM A SINGLE TERMINAL
  - COMMON HUMAN INTERFACE

● SYNTAX DRIVEN HUMAN INTERFACE, WITH ON-LINE HELP AND COMMAND LINE RECALL
DEBUG SUPPORT
ICE™ 386

- NON-INVASIVE HARDWARE DEBUG
- REAL-TIME DEBUGGING
- ADVANCED HUMAN INTERFACE
DEBUG SUPPORT

ICE™ 386

- 16 MHz EMULATION
- HIGH SPEED DOWNLOAD
- 128 BYTES OF ICE MEMORY
- 2K FRAME TRACE BUFFER
- DYNAMIC TRACE
- FAST BREAKS
ICE 386 HARDWARE

- CONSISTS OF TWO POWER SUPPLIES (ONLY ONE IN FUTURE)
- SAST (STAND ALONE SELF TEST)
  UNIT FOR RUNNING DIAGNOSTICS AND RUNNING STAND ALONE
- CU (CONTROL UNIT)
  DUAL PROCESSOR ICE DESIGN WITH 188.
  CONTAINS BREAK, TRACE, COMMUNICATION AND MEMORY.
- PROCESSOR MODULE (800 mA required from target)
  CONTAINS 80386 AND BUFFERS GOING BACK TO THE ICE
- SAB (SIGNAL ACCESS BOARD)
  PROVIDES EASY ACCESS TO 386 SIGNALS
- DIB OPTIONAL ISOLATION BOARD
  (500mA required from target)
  BUFFERS THE TARGET FROM THE 80386
  RUNS AT 8 MHZ
- RS 232 CONNECTOR FOR COMMUNICATION WITH THE HOST
- PM TO CU INTERFACE CABLE
- 488 INTERFACE FOR FUTURE RELEASE

CUSTOMER SUPPORT OPERATION
Figure 1-2 The ICE™-386 Components and the Intel System 286/310

CUSTOMER SUPPORT OPERATION
ICE 386 FEATURE SET

- Download code to target system
- 128K Uf mapable ICE memory
- Examine and modify memory, and registers
- Examine and modify descriptor tables
- Single stepping
- Disassembly of code in memory
ICE 386 FEATURE SET (CONT)

- Working C-like debugging procedures and macros
- Procedural and line stepping (PSTEP, LSTEP)
- Callstack frame analysis
- Virtual 86 support
- Single line assembler
- State machine breakpoints
- Load command for target memory
ICE 386 FEATURE SET (CONT)

- Execution Address Trace
- Emulation Timer for Timing Code
- Execution of Xenix Commands While in ICE 386
- Emulation up to 16 MHz
- Symbolics
DEBUG SUPPORT STARTER KIT

- MULTIBUS® I OR MULTIBUS® II CPU/MEMORY BOARD
- CABLES
- DOCUMENTATION
- PMON 386 MONITOR SOFTWARE

*XENIX IS A TRADEMARK OF MICROSOFT CORP.*
DEBUG SUPPORT
PscapeMONitor 386
(PMON 386)

- HOST SOFTWARE FOR HIGH LEVEL CONTROL
- FIRMWARE FOR 80386-BASED TARGET MONITORING
- CONFIGURABLE ON ANY 80386 TARGET SYSTEM
- PRE-CONFIGURED FOR 386/20 AND 386/100 BOARDS
DEBUG SUPPORT
PMON 386

- EXAMINE/MODIFY REGISTERS, MEMORY, AND I/O PORTS
- DOWNLOAD 8086, 80286, AND 80386 OBJECT MODULES
- SET ON-CHIP HARDWARE BREAKPOINTS
- SET SOFTWARE BREAKPOINTS
- CONTROL PROGRAM EXECUTION - “GO” AND “STEP”
- DISASSEMBLE MEMORY IN 80386 MNEMONICS
HOST FEATURES

- Can evaluate and use complex expressions
- Control constructs in a common programming language (C like macro set)
- Command procedures can be written
- Online help facility (not implemented)
- Command line editing and history buffer
- Syntax guide
- I/O redirection and piping
- Foreground/background jobs
- Host (Xenix/Unix/MSDos) program execution within RX
TOOL COMMAND LANGUAGE

- DISPLAY MODIFY TARGET DATA STRUCTURES
- MAINTAIN DEBUG OBJECTS FOR STURING LITERALS, VARIABLES OR PROCS
- CREATE AND EXECUTE COMMAND SEQUENCES
- DISPLAY MODIFY PROGRAM MEMORY USING SYMBOLICS
- EVALUATE PROGRAM MEMORY AND DATA TYPE EXPRESSIONS
- VIEW PROGRAM SYMBOLIC INFORMATION
SOFTWARE COMPATIBILITY
80386 SOFTWARE COMPATIBILITY
80386 SOFTWARE BASE

- 8086/8088 SOFTWARE
- 80286 SOFTWARE
- NEW 32-BIT SOFTWARE
80386 SOFTWARE COMPATIBILITY
FULL SOFTWARE POTENTIAL

- RUN 8086, 80286, NEW 32-BIT PROGRAMS CONCURRENTLY
- FULL 80386 PERFORMANCE DELIVERED TO ALL
- NO NEED FOR COMPLEX MULTIPROCESSOR, MULTIPLE-ARCHITECTURE DESIGN
80386 SOFTWARE COMPATIBILITY
8086 COMPATIBILITY

• VIRTUAL 8086 MACHINE
  - ALLOWS DIRECT EXECUTION OF 8086 SOFTWARE WITH
    PROTECTION
    MULTITASKING
    PAGED VIRTUAL MEMORY
80386 SOFTWARE COMPATIBILITY
VIRTUAL 86 MACHINE

- Allows direct execution of 8036 software
- Operates in protected mode
- Operates in paged (virtual memory) environment
- Enabled on a per-task basis
- Full 80386 performance

* MULTIMATE is a trademark of MULTIMATE INTL.
80386 SOFTWARE COMPATIBILITY
80286 SOFTWARE

- EXECUTES 80286 O.S. UNCHANGED
- EXECUTES 80286 APPLICATIONS UNCHANGED
- TWO ENVIRONMENTS:
  - 80286 SOFTWARE DIRECTLY ON 80386
  - 80286 SOFTWARE UNDER 80386 O.S.
80386 SOFTWARE COMPATIBILITY
80286 SOFTWARE UNDER 80386 O.S.

- RUNS UNCHANGED 80286 APPLICATIONS ON 32-BIT MACHINE
- SUPPORTED ON A PER-TASK BASIS
- FULL 80386 PERFORMANCE
EXECUTING 80286 PROTECTED MODE CODE ON THE 80386

DIFFERENCES FROM THE 80286

- ADDRESSES WHICH WRAP BEYOND THE 16M BYTE ADDRESS SPACE OF THE 80286 WILL APPEAR IN THE 17TH MEGABYTE OF 80386 ADDRESS SPACE.

- RESERVED WORD IN 80286 DESCRIPTORS MUST BE UNUSED TO EXECUTE CORRECTLY ON THE 80386.

- THE 80386 HAS ADDITIONAL DESCRIPTOR TYPE CODES OVER THE 80286. 286 OPERATING SYSTEMS WHICH USE RESERVED DESCRIPTOR TYPE CODES WILL LIKELY NOT RUN ON THE 80386.

- THE LOCK INSTRUCTION PREFIX USAGE IS MORE RESTRICTED ON THE 386.

- ADDITIONAL EXCEPTION CODES HAVE BEEN DEFINED FOR THE 80386.

  EXCEPTION #6 - INVALID OPCODE CAN RESULT FROM IMPROPER USE OF THE LOCK INSTRUCTION.

  EXCEPTION #14 - PAGE FAULT MAY OCCUR IF PAGING IS ENABLED WHILE A 286 TASK IS RUNNING. PAGING CAN ONLY BE USED WITH 286 CODE IF ALL 286 TASKS SHARE THE SAME PAGE DIRECTORY
EXECUTING 80286 PROTECTED MODE CODE ON THE 80386

LIMITATIONS OF RUNNING 80286 CODE ON THE 80386

* BASE ADDRESS - HIGH ORDER BYTE OF BASE ADDRESS MUST BE ZERO LIMITING BASE ADDRESSES TO 24 BITS

* LIMIT - THE HIGH ORDER FOUR BITS OF LIMIT FIELD ARE ZERO RESTRICTING LIMIT FIELD TO 64K

* GRANULARITY - GRANULARITY BIT MUST BE SET TO ZERO WHICH SETS LIMIT GRANULARITY TO ONE BYTE

* B-BIT - IN A DATA SEGMENT_DESCRIPTOR THE B-BIT IS ZERO IMPLYING NO SEGMENT LARGER THAN 64K

* D-BIT - IN AN EXECUTABLE SEGMENT_DESCRIPTOR THE D-BIT IS ZERO IMPLYING 16-BIT ADDRESSING AND OPERANDS ARE THE DEFAULT